REMARKS

Reconsideration of the application is requested.

Claims 11-20 remain in the application. Claims 11-20 are subject to examination. Claims 11-14, 16, 17, 19 and 20 have been amended.

Under the heading "Claims Rejections - 35 U.S.C. §101" on pages 2-3 of the above-identified Office Action, the Examiner objected to claims 12 and 16-19 for being inoperative. The Examiner states that the formula of claim 12 is erroneous and the formula in question is now reproduced.

$$Pist = V_S * I_S = Vdiffabs * d(Vdiffabs)/dt * C1,$$

where

Pist = power loss

Vdiffabs = absolute value of the difference voltage

V_S = switch voltage = Vdiffabs,

I_S = d(Vdiffabs)/dt*C1, and

C1 = const.

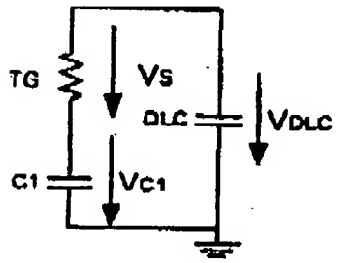
The Examiner's rejection is footed on the statement "It is true that the current in the case is determined as a derivative of the voltage (see formula at the bottom of

page 23), but it is the voltage across the capacitor and by no means, a potential difference across the resistive element, the semiconductor switch, as Applicant suggests."

We think the mathematical conclusions stated in claim 12 hold true for the now described reasons.

The relation between a current Ic_1 through a capacitor C1 and the derivative of the voltage Vc_1 across capacitor C1 is described as

(1) $Ic_1 = C1 * d(Vc_1)/dt$.



This figure is an abstraction of Fig. 2 shown in the instant application.

As described on page 2, lines 5-9 of the specification, the value of the double layer capacitor DLC is orders of magnitude larger than the value of capacitor C1 (200F vs. 10.000μF). Therefore, charging C1 from 0V to V_{DLC} will

render V_{DLC} unchanged due to technical purposes (e.g. DLC storing significantly greater energy than needed to charge C1). Hence the DLC can be seen as having an almost ideal voltage source for this consideration.

As shown in figure above, the voltage across the DLC equals the sum of the voltages across the resistive element TG and the capacitor C1.

{2} $V_{DLC} = V_s + V_{C1}$

or

{2a} $V_{C1} = V_{DLC} - V_s$

Inserting {2a} into formula {1} yields

{3} $Ic_1 = C1 * d(V_{DLC} - V_s)/dt$

or

{3a} $Ic_1 = C1 * d(V_{DLC})/dt - C1 * d(V_s)/dt.$

Since the voltage V_{DLC} does not change as described above, its derivative is zero.

$d(V_{DLC})/dt = 0$, as well as $C1 * d(V_{DLC})/dt = 0$

This reduces (3a) to

(3b) $Ic_1 = - C1 * d(V_s)/dt$

Further more, the current flowing through C1 is also flowing through TG and therefore

(4) $Ic_1 = I_s$.

Inserting (4) into (3b) finally yields

(5) $I_s = - C1 * d(V_s)/dt$.

This is - <u>besides the difference in sign</u> - exactly what has been recited in the formula of claim 12.

The difference in sign of I_s is negligible for the given purpose, since Pist has a positive sign per definition (there cannot be a negative power loss).

In summary:

- V_{DLC} is constant; and

- If V_{C1} has a change rate of 1V/s, then Vs will have a change rate of -1V/s. That is, both derivatives have the same value, but opposite signs.

It is in fact very easy to determine V_{C1} and calculate its derivative. However, since Vs needs to be sensed anyway, the effort can be spared.

For the above stated reasons, the Examiner is requested to withdraw the 35 U.S.C. §101 rejection.

As the Examiner notes the term "differential voltage" is indeed confusing and is now recited as a "difference voltage" throughout the claim language to move away from confusion with the term "differential".

Under the heading "Claim Rejections - 35 USC § 112" on pages 3-4 of the above-identified Office Action, claims 12 and 20 have been rejected as being indefinite under 35 U.S.C. § 112, first or second paragraphs.

More specifically, the Examiner states that with regard to claim 20, paragraph [0048] of the specification

contradicts claim 20. Paragraph [0048] relates to Fig. 5. The Examiner is respectfully directed to Fig. 8 and paragraphs [0061 and 0062] for a more comprehensive understanding of claim 20.

With regards to claim 12, the Examiner notes a positioning issue with the formula. Claim 12 has been amended to position the formula in a more appropriate spot, namely to be associated with the multiplying step rather the differentiating step.

It is accordingly believed that claims 12 and 20 meet the requirements of 35 U.S.C. § 112, first and second paragraph. The above-noted changes to the claims are provided solely for clarification or cosmetic reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

Under the heading "Specification" on page 4 of the Office Action, the Examiner objects to paragraphs [0011, 0012 and 0017]. The offending paragraphs have been deleted from the application.

Under the heading "Claim Rejections - 35 USC § 102" on pages 5-6 of the above-identified Office Action, claims 11 and 13 have been rejected as being fully anticipated by U.S. Patent No. 6,347,028 to Hausman et al. (hereinafter Hausman) under 35 U.S.C. § 102.

In the instant application, the transfer gate TG (Figs. 2 and 3) is controlled by impressing a control voltage Vst between the gate terminals and the source terminals of the two transistors Q1 and Q2 of the transfer gate TG. The control voltage Vst sets the degree of conductance of the FETs Q1, Q2 and therefore continuously controls the voltage drop (difference voltage) between the terminals E and A (vdiff) in a continuous manner. One can control the control voltage Vst for maintaining a desired continuously power loss across the transfer gate. A constant or clamped power loss must be contrasted with an emergency shut down condition as is performed by an overcurrent protection circuit. In other words, the power loss in the instant application is continuously clamped at a set desired value and the circuit breaker continuously operates at the predetermined setpoint should the current be sufficient to reach this value by continuously modifying the conductance rate of the FETs. Claims 11 and 14 have been amended to support Applicants' argument. As

shown in Fig. 3, the control voltage Vst is impressed between the gate terminal and the source terminal and as noted on page 3, lines 1-26 of the specification, the power loss is kept constant (regulated) at the predetermined setpoint. In addition, support comes from claim 12, last paragraph.

In contrast, Hausman teaches an overload circuit 36 for monitoring an overcurrent condition across FETs Q1 and Q2. When an integrated value of the voltage across the FETs Q1, Q2 exceeds a predetermined threshold the FETs are put in a non-conducting state by controlling the voltage supplied only to the gate terminals. In order to determine the power loss across the FETs an average voltage V_{avg} across the FET is compared to a variable threshold V_{th}. The variable threshold V_{th} is determined by the ON-state resistance R_{DS} of the FET and is temperature sensitive. Please note that Hausman teaches only to monitor the voltage across the FETs Q1, Q2 and to shut them off in an overcurrent condition. The FET is turned off by cutting off any voltage impressed on the gate terminals of the FETs. Please note that Hausman does not teach any feedback for controlling the on-going operation of the FETs and limiting a continuous operation at a desired power loss. In other words, the current to the

control gate is off or on, but it is not continuously regulated for continuously modifying a conductance rate. There is only the state of an off or on and not a state of varying the conductance for clamping the voltage to a set power loss as in the instant application.

Under the heading "Claim Rejections - 35 USC § 103" on pages 6-7 of the above-identified Office Action, claims 14, 15 and 20 have been rejected as being obvious over U.S. Patent No. 6,347,028 to Hausman et al. (hereinafter Hausman) in view of U.S. Patent No. 5,640,293 to Dawes (hereinafter Dawes) and further in view of U.S. Patent No. 6,828,755 to Iverson et al. (hereinafter Iverson) under 35 U.S.C. § 103.

As noted above, claim 14 was amended to overcome Hausman and the incorporated features from Dawes and Iverson do not teach the newly added feature that the circuit breaker can continuously operate at the predetermined setpoint and regulates the power loss to the predetermined setpoint.

In addition, in Hausman, it is only the voltage impressed between the gate terminal and ground that is controlled. In contrast in amended claim 14, the control voltage is

impressed between the gate and source terminals for controlling the FETs.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 11 and 14. Claims 11 and 14 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 11 or 14.

In view of the foregoing, reconsideration and allowance of claims 11-20 are solicited.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $120.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account

of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

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REL:cgm

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